Amendments to the Specification:

On the Title Page:

Please amend the paragraph beginning on line 3 of the title page to read as follows.

This is a divisional of U.S. application Serial No. 09/795,487, filed March 1, 2001, now U.S. Patent No. 6,759,338, the subject matter of which is incorporated by reference herein.

Page 8, amend the paragraph beginning on line 12 to read as follows:

The electrode arrangement 3 for mounting a wafer 21 is composed of an electrode 22 which is made of aluminum and an alumina film 22A which is coated by sputtering on the surface of the electrode 22. The alumina film 22A is coated at a thickness such that the thickness at the ring portion 23A, i.e. a part outside of its inner part having a diameter of two thirds of the electrode diameter, is three times of the thickness at the inner part. Also, an electrode 23 of tungsten is buried at the ring portion 23A at a depth of one thirds of the thickness of the electrode from its surface and connected to a feeder line 24 which is insulated from the electrode material. This feeder line 24 is connected through a variable capacitor 25, together with the electrode to a bias power source circuit 26. The variable capacitor 25 is capable of being either short-circuited or opened and having a capacity variable from infinite to zero.

Page 8, amend the paragraph beginning on line 25 to read as follows:

Further, the silicon ring 27 has an outer diameter of 1.5 times of the wafer diameter and is disposed on the electrode 22. The thickness of the alumina film 22B

at a portion where the silicon ring 27 is disposed is two times of the thickness of its center portion. In the insulating alumina film 22B, an electrode 28 of tungsten is buried and connected to the electrode material through a feeder line 29 and a variable capacitor 30.

Page 10, amend the paragraph on line 20 to read as follows:

This is because the bias impedance is reduced at positions opposing to the plasma main generating positions within the wafer surface and thereby the potential produced by the bias is varied depending on the positions on the wafer surface. In this case, as shown in Fig. 10, by disposing the portion 41A, where the thickness of the alumina is larger than other portions and the electrode 41 is embedded, at a position opposing to the plasma main generating position and adjusting the capacitance of the variable capacitor 43, it is possible to reduce the rate of defective chips due to charging damages to 0 %. Incidentally, in Fig. 10, 42 is a feeder line, 44 and 45 are resonance coils, 46 a bias high frequency power source, and 47 a variable D.C. power source.